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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/789,025	01/27/1997	JOSEPH KERZMAN	33012/184/10	8513

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EXAMINER
JONES, HUGH M

ART UNIT	PAPER NUMBER
2123	16

DATE MAILED: 02/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Notification of Non-Compliance with 37 CFR 1.192(c)

Application No.	Applicant(s)
08/789,025	Kerzman et al.
Examiner	**Art Unit**
Hugh Jones	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

The Appeal Brief filed on *Jan 28, 2002* is defective for failure to comply with one or more provisions of 37 CFR 1.192(c). See MPEP § 1206.

To avoid dismissal of the appeal, applicant must file IN TRIPLICATE a complete new brief in compliance with 37 CFR 1.192(c) within the longest of any of the following three TIME PERIODS: (1) ONE MONTH or THIRTY DAYS from the mailing date of this Notification, whichever is longer; (2) TWO MONTHS from the date of the notice of appeal; or (3) within the period for reply to the action from which this appeal was taken. EXTENSIONS OF THESE TIME PERIODS MAY BE GRANTED UNDER 37 CFR 1.136.

1. ☐ The brief does not contain the items required under 37 CFR 1.192(c), or the items are not under the proper heading or in the proper order.

2. ☐ The brief does not contain a statement of the status of all claims, pending or cancelled, or does not identify the appealed claims (37 CFR 1.192(c)(3)).

3. ☐ At least one amendment has been filed subsequent to the final rejection, and the brief does not contain a statement of the status of each such amendment (37 CFR 1.192(c)(4)).

4. ☒ The brief does not contain a concise explanation of the claimed invention, referring to the specification by page and line number and to the drawing, if any, by reference characters (37 CFR 1.192(c)(5)).

5. ☐ The brief does not contain a concise statement of the issues presented for review (37 CFR 1.192(c)(6)).

6. ☐ A single ground of rejection has been applied to two or more claims in this application, and

   (a) ☐ the brief omits the statement required by 37 CFR 1.192(c)(7) that one or more claims do not stand or fall together, yet presents arguments in support thereof in the argument section of the brief.

   (b) ☐ the brief includes the statement required by 37 CFR 1.192(c)(7) that one or more claims do not stand or fall together, yet does not present arguments in support thereof in the argument section of the brief.

7. ☐ The brief does not present an argument under a separate heading for each issue on appeal (37 CFR 1.192(c)(8)).

8. ☐ The brief does not contain a correct copy of the appealed claims as an appendix thereto (37 CFR 1.192(c)(9)).

9. ☒ Other (including any explanation in support of the above items):

   Please note enclosed pages 6, 9, 37 and 42 of the specification.

DETAILED ACTION

NOTIFICATION OF NON-COMPLIANCE WITH THE REQUIREMENTS OF 37 CFR 1.192(c)

1. This communication is responsive to the Third Supplemental Appeal Brief filed 1/28/2002.

2. The brief does not contain a concise explanation of the invention ***defined in the claims*** involved in the appeal, ***which refers to the specification by page and line number***, and to the drawing, if any, by reference characters as required by 37 CFR 1.192(c)(5). Appellants have a detailed statement where the *claim limitations* are supported in the specification and/or incorporated co-pending Applications and Appellants are thanked for the specific references to portions of the specification as evidence of support for the claims. However, the Examiner has reviewed said mapping and notes the following.

3. Most of the indicated support still refers to *fragments* of sentences and paragraphs. For example, Appellants refer (pages 16-17, paper # 15) to the specification as evidence of support for the following:

- claim 1, limitation b: Appellants refer to page 37, lines 4-8, fig. 4, # 206;
- claim 2: page 42, lines 6-10;
- claims 4, 19-20, 30: page 9, lines 16-18;
- claims 10, 35: page 6, lines 5-10;
- claims 11, 36: page 9, lines 11-13

4. The Examiner has reviewed the indicated sections and notes that the portions are fragments of sentences and paragraphs which do not even indirectly relate to the claimed feature. Note, also, that pages 6 and 9 are contained in the section entitled "*Backround of the invention.*" The Examiner has provided repeated and sufficient notice to Appellants regarding this issue. Furthermore, the material on pages 37 and 42 appear to refer to incorporated material. Enclosed with the Official Office Action are pages 6, 9, 37 and 42 from Applicant's specification, as per the above discussion.

5. Appellant is required to comply with provisions of 37 CFR 1.192(c).

6. To avoid dismissal of the appeal, Appellant must comply with the provisions of 37 CFR 1.192(c) within the longest of any of the following TIME PERIODS: (1) ONE MONTH or THIRTY DAYS, whichever is longer, from the mailing of this communication; (2) within the time period for reply to the action from which appeal has been taken; or (3) within two months from the date of the notice of appeal under 37 CFR 1.191. Extensions of these time periods may be granted under 37 CFR 1.136.

7. **Any inquiry concerning this communication or earlier communications from the examiner should be:**

directed to: Dr. Hugh Jones telephone number (703) 305-0023, Monday-Thursday 0830 to 0700 ET, ***or*** the examiner's supervisor, Kevin Teska, telephone number (703) 305-9704. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

mailed to: Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 308-9051 (for formal communications intended for entry) ***or***

(703) 308-1396 (for informal or draft communications, please label "*PROPOSED*" or "*DRAFT*").

Dr. Hugh Jones

February 9, 2002

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER

in section "Background of the Invention"

during the integrated circuit design process, because errors may be detected during the simulation and testing phases of the design cycle and then fixed in the behavioral description.

The output of the design capture and synthesis tools is a logic design database which completely specifies the logical and functional relationships among the components of the design. Once the design has been converted into this form, it may be optimized by sending the logic design database to a logic optimizer tool implemented in software. The logic optimizer may remove logic from the design that is unnecessary, or otherwise improve the overall efficiency of the design. It is noted, however, that this action typically affects the component and net names generated by the logic synthesis tool.

Claims 10, 35

It is also necessary to verify that the logic definition is correct and that the integrated circuit implements the function expected by the circuit designer. This verification is currently achieved by estimated timing and simulation software tools. The design undergoes design verification analysis in order to detect flaws in the design. The design is also analyzed by simulating the device resulting from the design to assess the functionality of the design. If errors are found or the resulting functionality is unacceptable, the designer modifies the behavior description as needed. These design iterations

"Background of the Invention"

Likewise, if a design rule violation is detected, a physical database editor may be used to edit the physical database to correct the violation.

In all of the above cases, it may be important to view specific pre-identified cells or components that are involved in the detected errors. Once a circuit designer can view an offending cell, an editing function of the database editor tool may be used to correct the violation.

In prior art database editor tools, this correction process could be tedious and time-consuming because there was not an efficient method for locating the cells or nets involved in the violations. A circuit designer typically had to manually locate the violations by panning through the design using the database editor's graphics window. Even when the exact location of the violation was known, navigating to that location could be slow, particularly since the graphics terminal may be manipulating files that contained tens of thousands of objects. Further, once the violation was found, the database editor was not set to the proper level in the design hierarchy to immediately allow an editing function on the offending cell or component.

Claims 30, 19, 20, 4

this is "Background of the Invention" 9 Claims 36, 11

"Method and Apparatus for Resolving Conflicts Between Cell Substitution Recommendations Provided by a Drive Strength Adjust Tool, which has been incorporated herein by reference.

After all conflicts are resolved, the second merging step 208 may provide a final substitution list. In the exemplary embodiment, the final substitution list is provided to a floorplan tool 168 (e.g., CHIPLAN) via interface 210. The designer may then make the necessary modifications to the design database. Thereafter, the design database may be provided to the place and route tool, for final placement and routing. The exemplary method may then be exited (not shown), or the process may be repeated to verify that the design database meets the circuit design specification.

Claim 1, element "b"

110 may read the floorplan file 108 directly via interface 160. This may allow the physical violations checker 110 to detect violations in the floorplan file 108, without first performing a cell substitution. This may be particularly useful when the physical violations checker 110 can detect violations other than those caused by cell substitutions.

In some cases, a cell substitution may cause the performance of the design to decrease or otherwise not have the intended effect. Under these circumstances, it may be desirable to undo the cell substitutions made by cell substitution block 102, and revert back to a previous design iteration. A reset database block 152 may be provided to accomplish this task. The reset database block 152 may read the floorplan file 108, and may reset the floorplan file 108 back to a previous state. The set cell list 96 may then be exported and used by a drive strength adjust tool, as the basis for a new cell substitution. An exemplary drive strength adjust tool is discussed in U.S. Patent Application Serial No. 08/598,506, filed on February 7, 1996, and entitled "Method and Apparatus for Performing Drive Strength Adjust Optimization in a Circuit Design".

A number of features may be incorporated into the data processing system to aid in the placement of the design database 94. A context control block 116 may read the floorplan file 108 via interface 118, and may set the current context to a selected hierarchical level. A context